What is claimed is:

1. A circuit comprising:

an operation unit adapted to perform a circuit operation in a plurality of rounds, the operation unit to operate properly under a predetermined range of operating conditions, the operation unit adapted to select between receiving an input signal and a test signal and to perform a test round of the circuit operation when the test signal is selected;

the circuit adapted to compare a reference value with a result of the test round, the reference value identifying a correct value for the result of the test round when the operation unit is operating under the predetermined range of operating conditions; and

the operation unit further adapted to receive a disable signal to disable the operation unit from performing the circuit operation, the disable signal produced when the result of the test round does not match the reference value.

2. The circuit of claim 1 in which the circuit operation comprises one of an encryption of decryption operation.

3. The circuit of claim 1 in which the operation unit is further adapted to receive a test key signal and to perform the test round applying the test key signal and the test signal in response to a first clock signal, the circuit adapted to compare the reference value with the result of the test round in response to a subsequent clock signal, the operation unit adapted to select the input signal and perform a first round of the plurality of rounds of the circuit operation applying the input signal in response to the subsequent clock signal.

4. A method comprising:

selecting a test signal to apply to a test round of a circuit operation, the circuit operation comprising a plurality of rounds;

comparing a result of the test round with a stored reference value, the stored reference value identifying a correct value for the result of the test round when the circuit is operating under a predetermined range of operating conditions; and

producing a disable signal to disable the operation unit from performing the circuit operation when the result of the test round does not match the reference value.

5. The method of claim 4 in which selecting the test signal further comprises:

selecting the test signal and a test key signal to perform one of an encryption or decryption operation by applying the test key signal to the test signal.

6. The method of claim 4 in which in which selecting the test signal further comprises:

selecting the test signal and a test key signal; and

performing the test round applying the test key signal and the test signal in response to a first clock signal.

7. The method of claim 4 in which comparing the result of the test round with a stored reference value further comprises:

selecting an input signal in response to a subsequent clock signal; and

comparing the result of the test round with a stored reference value in response to a subsequent clock signal and performing a first round of the plurality of rounds of the circuit operation in response to the subsequent clock signal.

8. A circuit comprising:

a sampling unit to produce a measure of a first frequency of a clock signal applied to the circuit;

a memory to store the measure of the first frequency; and

an analytical unit to compare the measure of the first frequency with a measure of a second frequency of the clock signal applied to the circuit, the analytical unit adapted to produce a disable signal to disable the circuit when a difference between the measure of first frequency and the measure of the second frequency exceeds a threshold value.

9. The circuit of claim 8 in which the sampling unit further comprises:

an oscillator adapted to produce a frequency greater than the first and second frequencies of the clock signal; and

a counter to count a number of oscillations of the oscillator during a period of the clock signal.

10. The circuit of claim 9 in which the counter comprises a Johnson counter.

11. The circuit of claim 9 in which the analytical unit further comprises:

a subtractor to determine the difference between the measure of first frequency and the measure of the second frequency.

12. The circuit of claim 11 in which the analytical unit further comprises:

a magnitude comparator to receive the difference between the measure of the first frequency and the measure of the second frequency and to produce the disable signal when the difference exceeds a threshold value.

13. A method comprising:

sampling a clock signal applied to a circuit to produce a first frequency sample;

storing the first frequency sample;

again sampling the clock signal to produce a second frequency sample;

comparing the first frequency sample with the second frequency sample; and

producing a disable signal to disable the circuit when the difference between the first frequency sample and the second frequency sample exceeds a threshold value.

14. The method of claim 13 further comprising:

producing an oscillation comprising a frequency greater than the frequency of the clock signal; and

counting a number of oscillations during a period of the clock signal.

15. The method of claim 13 in which sampling the clock signal further comprises:

producing the first frequency sample during the clock signal when applied to the circuit at a start of a circuit operation; and

producing the second frequency sample during the clock signal when applied to the circuit during the circuit operation.